

CLAIMS

What is claimed is:

1 1. An integrated circuit chip with redundant elements, comprising:
2 a substrate die;
3 a plurality of microprocessors disposed in said substrate die, each microprocessor
4 having a data interface;
5 a plurality of cache memories disposed in said substrate die, each cache memory
6 having at least one memory interface for accessing the cache memory; and
7 a signal bus disposed in said substrate die, said signal bus including a programmable
8 selector circuit for selecting a subset of said plurality of microprocessors to be
9 used for processing information and for selecting a subset of said plurality of
10 cache memories, said selector circuit simultaneously linking the data interface
11 of a first selected microprocessor to a memory interface of a first selected
12 cache memory and linking the data interface of a second selected
13 microprocessor to a memory interface of a second selected cache memory.

1 2. The integrated circuit chip of Claim 1, wherein the substrate die comprises a
2 conductive silicon substrate having at least one bulk region and at least one silicon-on-insulator
3 region, the cache memories being dynamic random access memories residing on said at least one
4 bulk region and the microprocessors residing on said at least one silicon-on-insulator region.

1 3. The integrated circuit chip of Claim 1, wherein said signal bus is a broadband
2 signal bus.

1 4. The integrated circuit chip of Claim 1, wherein said signal bus further comprises
2 at least one active element to regenerate a data signal coupled by the signal bus between the first
3 selected microprocessor and the first selected cache memory.

1 5. The integrated circuit chip of Claim 1, wherein the chip is a multiprocessor and
2 there are a total of N microprocessors and a subset of N-1 microprocessors is selected for parallel
3 processing by the selector circuit.

1 6. The integrated circuit chip of Claim 5, wherein there are a total of N cache
2 memories and said selector circuit selects subset of N-1 cache memories for parallel processing.

1 7. The integrated circuit chip of Claim 5, wherein said cache memories are level-2 cache
2 memory units.

1 8. The integrated circuit chip of Claim 7, wherein one of said cache memories
2 comprises a cache sized to provide the cache resources of a level-2 cache memory and a level-3
3 cache memory.

1 9. The integrated circuit chip of Claim 1, wherein the chip is a multiprocessor and
2 the signal bus couples the microprocessors as a parallel processor.

1 10. The integrated circuit chip of Claim 9, wherein said plurality of microprocessors
2 includes at least nine microprocessors.

1 11. The integrated circuit chip of Claim 1 wherein said programmable selector circuit
2 is a multiplexor circuit.

1 12. The integrated circuit chip of Claim 1, wherein said cache memories include level-2
2 cache memories and level-3 cache memories and one microprocessor is coupled to one level-2
3 cache memory and to one level-3 cache memory by the signal bus.

1 13. A multiprocessor chip, comprising:

2 a silicon substrate die having at least one bulk region and at least one silicon-on-insulator
3 region, the silicon-on-insulator region including a buried oxide layer residing
4 a preselected distance between an outer surface layer of crystalline silicon;

5 a plurality of microprocessors, each said microprocessor formed in said at least one
6 silicon-on-insulator region, each microprocessor having a data interface;

7 a plurality of dynamic random access memory (DRAM) cache memories formed in said
8 at least one bulk region, each cache memory having a memory interface for
9 accessing the cache memory; and

10 a high bandwidth signal bus formed on said substrate having interconnect wires for
11 linking the data interface of one microprocessor to a corresponding memory
12 interface of one of the cache memories as a parallel processor.

1 14. The multiprocessor of Claim 13, wherein said signal bus includes a programmable
2 selector circuit for selecting a subset of the components that are utilized by the parallel processor,
3 whereby a defective component may be bypassed, the selected components being chosen from a
4 group consisting of microprocessors, cache memories, and the interconnect wires of the signal
5 bus.

1 15. The multiprocessor of Claim 13, wherein said cache memories are comprised of
2 trench DRAM memories.

1 16. The multiprocessor of Claim 15, wherein said buried oxide layer has a thickness
2 of less than 200 nanometers.

1 17. The multiprocessor of Claim 16, further comprising a layer of ions disposed
2 proximate the interface of the buried oxide layer and the surface layer of crystalline silicon, said
3 ions having a polarity and dose selected to suppress backgate conduction.

1 18. The multiprocessor of Claim 13, wherein said signal bus includes at least one
2 active element to regenerate a signal coupled between a microprocessor and a cache memory.

1 19. The multiprocessor of Claim 13, wherein one of the cache memories is a level-2
2 cache memory.

1 20. The multiprocessor of Claim 13, wherein one of the cache memories has a data
2 capacity sufficient to provide the function of a level-2 cache memory and a level-3 cache
3 memory.

1 21. The multiprocessor of Claim 13, wherein the cache memories comprise level-2 cache
2 memories and level-3 cache memories.

1 22. A multiprocessor chip, comprising:

2 a silicon substrate die having at least one bulk region and at least one silicon-on-insulator
3 region, the silicon-on-insulator region including a buried oxide layer residing
4 a preselected distance below an outer surface layer of crystalline silicon;

5 a plurality of microprocessors, each said microprocessor formed in said at least one
6 silicon-on-insulator region, each microprocessor having a data interface;

7 a plurality of dynamic random access memory (DRAM) level-2 cache memories formed
8 in said at least one bulk region, each level-2 cache memory having a memory
9 interface for accessing the memory; and

10 a high bandwidth signal bus formed on said substrate die having interconnect wires for
11 linking the data interface of one microprocessor to a corresponding memory
12 interface of one of the level-2 cache memories as a parallel processor, said
13 signal bus including a programmable selector circuit for selecting a subset of
14 said plurality of microprocessors and for selecting a subset of said cache
15 memories to be used for parallel processing, said selector circuit
16 simultaneously linking the data interface of a first selected microprocessor to
17 the memory interface of a first selected cache memory and linking the data
18 interface of a second selected microprocessor to the memory interface of a
19 second selected cache memory, whereby a defective microprocessor or a
20 defective cache memory may be bypassed.

1 23. The multiprocessor chip of Claim 22, wherein the level-2 cache memories are sized
2 to provide the function of off-chip level-2 cache memories and off-chip level-
3 3 cache memories.

1 24. The multiprocessor chip of Claim 22, further comprising:

2 a second plurality of dynamic random access memory (DRAM) cache memories formed
3 in said at least one bulk region, each cache memory of the second plurality of
4 cache memories sized to provide the function of a level-3 cache memory and
5 having a memory interface for accessing the memory, wherein said second
6 plurality of cache memories is simultaneously coupled by said signal bus to
7 the plurality of microprocessors with a first selected microprocessor linked to
8 a first selected one of the second plurality of cache memories and with a

9 second selected microprocessor linked to a second selected one of the second
10 plurality of cache memories.

1 25. A method of forming a multiprocessor chip on a silicon substrate, comprising the
2 steps of:

3 a) masking the substrate to form masked and unmasked regions;

4 b) implanting said substrate with an oxygen ion implant having an energy and dose
5 selected to form an implanted region underneath the surface of the substrate in
6 the unmasked regions and bulk regions in the masked regions;

7 c) annealing said substrate to form silicon-on-insulator in said implanted region;

8 d) forming dense microprocessors in said implanted region via deep ultraviolet
9 lithography;

10 e) forming dynamic random access memory units in the bulk region of said substrate; and

11 f) forming a signal bus for coupling said memory units to said microprocessors via a
12 signal bus.

1 26. The method of Claim 25, further comprising the step of implanting a backgate
2 conduction suppression charge layer proximate the interface of the silicon dioxide and the
3 surface layer of crystalline silicon to suppress parasitic backgate conduction.